# 5-GHz 20-WATT GaAs FET AMPLIFIER FOR MLS

K.Hirai, H.Takamatsu, S.Morikawa and N.Tomita

Microwave Solid-State Department
Komukai Works, Toshiba Corporation
1 Komukai-Toshiba-Cho, Saiwai-ku, Kawasaki, 210 Japan

## ABSTRACT

5-GHz 20-watt GaAs FET amplifier using two state-of-the-art high power FETs in the final stage was developed for MLS applications. GaAs FET limiter with unique input/output characteristics and efficient operation of the final FETs were studied for this purpose. Stabilization of output power within 1dB peak-to-peak was achieved by means of open loop control of PIN diode attenuator.

## INTRODUCTION

In Microwave Landing System (MLS), 5-GHz 20-watt GaAs FET amplifiers are used for both azimuth and elevation beam transmitter. The RF output power of 20 watts is given by combinations of four power FETs in the final stage. As the efficient RF power combining is the prime requirement, lowloss suspended strip transmissionline is used to make the power combiner, output filter, etc.

Recent progress in power FET technology, however, has brought about higher output power device which delivers more than 20 watts at 5GHz (1). The purpose of this paper is to report on the amplifier for MLS usung such state-of-the-art high power FETs. In addition to the description of the amplifier performance, techniques used to satisfy such tight system requirements as efficient DC-to-RF conversion, RF output power stabilization against ambient temperature change, lower noise output at key-off state, etc, are also presented.

## AMPLIFIER BLOCK DIAGRAM

The amplifier amplifies 5GHz input signal up to the power level of 20 watts with 30dB gain. It is a five stage GaAs FET amplifier. The first stage is a GaAs FET limiter to deliver constant RF power to the following linear amplifier stages regardless the change in input signal power level.

Two PIN attenuators are inserted between stages. The one is used for RF output power set, and the other for output power stabilization against ambient temperature change.

The RF output power of 20 watts is delivered from two high power FETs operat-

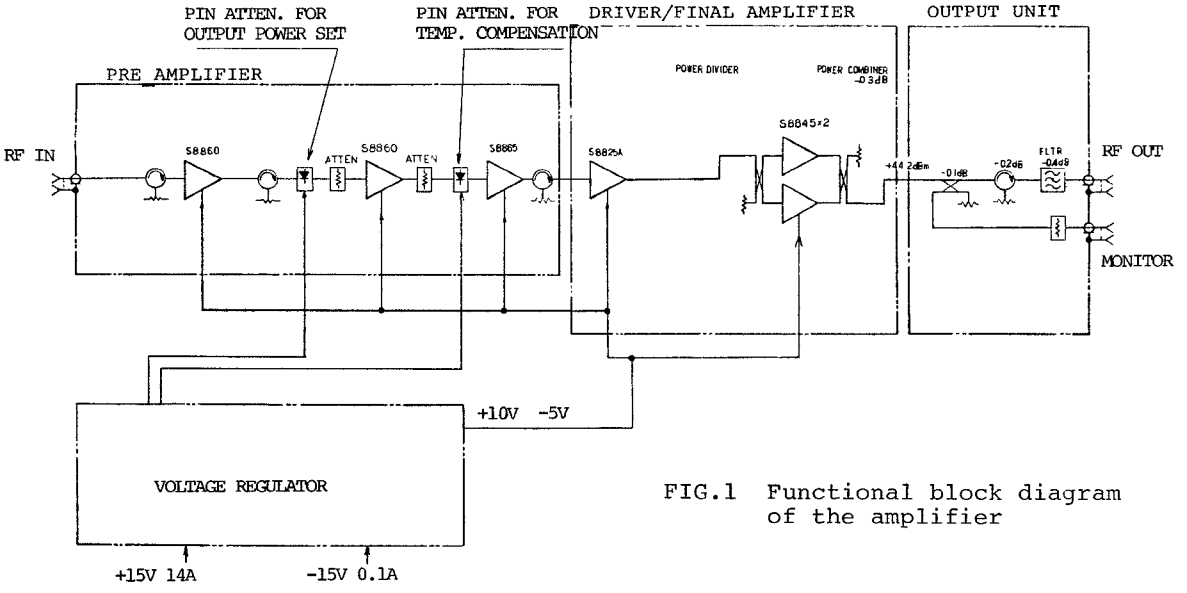



FIG.1 Functional block diagram of the amplifier



0149-645X/86/0000-0447$01.00 © 1986 IEEE

ing in parallel, through an isolator and a harmonic rejection filter.

## GaAs FET LIMITER

GaAs FET limiter gives stable RF output against change in RF input power and ambient temperature. When pulsed RF signal is applied, however, it generally brings about deterioration in on/off ratio because it acts as a linear, high gain amplifier for off-state low level signal.

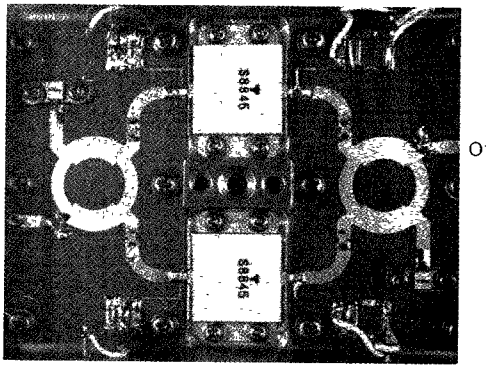
The important feature of the limiter used in this amplifier is its unique input/output characteristics to overcome the drawback of the conventional limiter. As shown in FIG.2, it has considerable gain and delivers saturated RF power for the RF input power range used, while it has little gain for smaller RF input power. When there is no incident RF power, the gate is biased to draw much current and reduce drain voltage below 0.5 volts due to the potential drop across the resistor in drain bias circuit. In this condition FET shows little gain. As RF input increases, gate voltage changes so as to reduce drain current and hence to increase drain voltage . Then FET shows considerable gain and delivers saturated output power for larger RF input.

This type of limiter is very advantageous to reduce the gain compression in the limiter and to reduce the noise power output during no RF input (key off) periods.

## FINAL AMP STAGE

Power FET in the final stage is Toshiba S8845, 20 watt device with 0.75μm gate length and 57.6mm gate width. As the amplifier is drived by long pulses in MLS application, class-B operation of the FETs is very attractive from the view of DC power saving(2). Therefore performance of the final stge amplifier is studied in detail taking the gate bias voltage as a parameter.

The experimental amplifier is shown in FIG.3(a). Measurements were done in the pulsed RF operation of 10ms pulse width and 50% duty ratio. Gate bias voltage (Vgs)




(a)

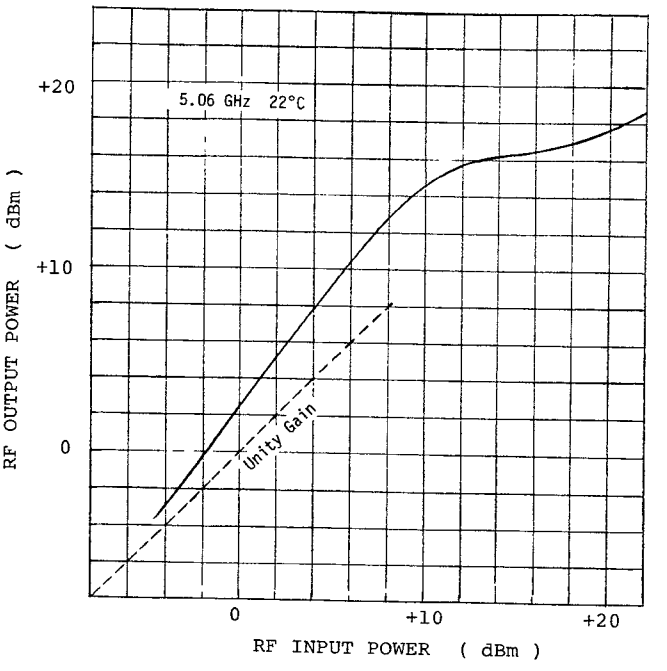



FIG.2 Input/output characteristics of the FET limiter

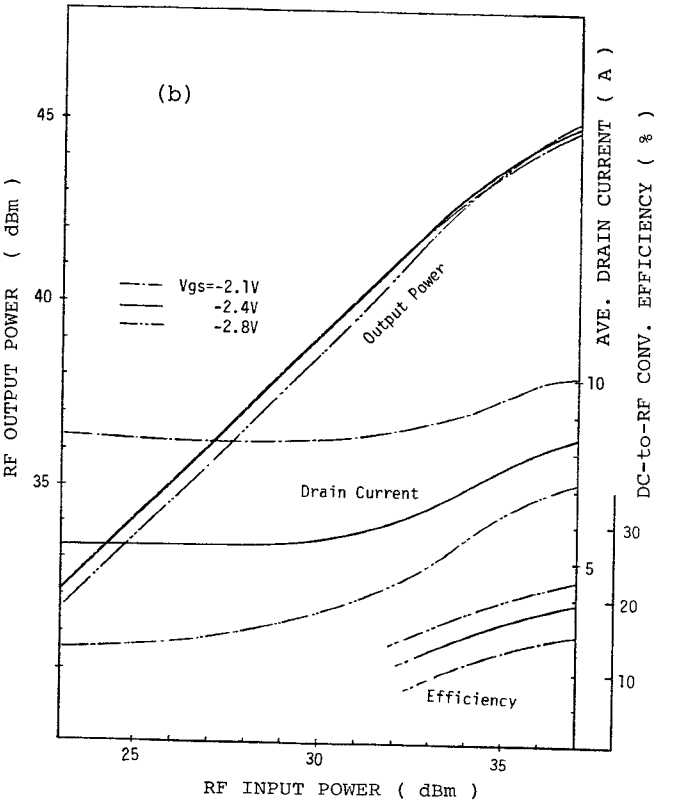



FIG.3 (a) Experimental final stage amplifier (b) Peak output power, average drain current and efficiency versus input power at 5.06GHz for the final stage amp.

was chosen -2.1, -2.4 and -2.8 volts considering the gate pinch-off voltage of 3.0 volts. Results are summarized in FIG. 3(b) with respect to RF input/output characteristics, average drain current and efficiency (average added RF power/average DC power input). The efficiency was increased by 50% for the near pinch-off gate bias voltage.

When gate is biased near pinch-off, abrupt change in drain current at the application of RF signal induces large transient voltage due to the inductance of wires between primary DC power supply and drain electrodes. Therefore large capacitance must be provided near drain electrode to remove the effect. Abrupt change in channel temperature also occurs which results in droop of the RF pulse envelope.

FIG.4(a), (b) and (c) show the trace of the RF pulse envelope at the pulse leading edge at 25°C for Vgs=-2.1V, -2.4V and -2.8V, respectively. When the ambient temperature was decreased to -50°C, significant swing of the amplitude was observed, as shown in FIG.4(d), (e) and (f), due to the degradation of dissipation factor of the 140μF capacitor at the drain bias terminal.

From the compromise between efficiency and RF output pulse distortion, gate bias voltage was set -2.4 volts.

## OUTPUT POWER STABILIZATION

As the amplifier must operate in tight temperature environment like -50 to +70°C, some means are required to stabilize output power. A PIN attenuator was used for this purpose.

Junction voltage of a PN diode with constant current drive was used to sense the amplifier baseplate temperature. The voltage was fed through an operational amplifier to PIN diodes so as just to compensate the gain variation of the amplifier with temperature. Closed loop control was not adopted because of the circuit complexity.

## HARMONIC REJECTION

Although final power FETs operate in almost linear input/output characteristic region, they generate considerable amount of harmonics. Microstrip harmonic rejection filter was realized with combinations of simple quarter-wavelength stubs at harmonic frequencies. Frequency response of the filter is shown in FIG.5. Harmonic outputs were suppressed below -53 dBc for the second and third harmonics, and below -83dBc for other harmonics.

## AMPLIFIER PROTECTION

The amplifier is protected against fully reflective load by preparing an isolator at the output port. It is also protected by the transistor switch inserted between DC power supply and FET drain terminals. The switch is activated in case

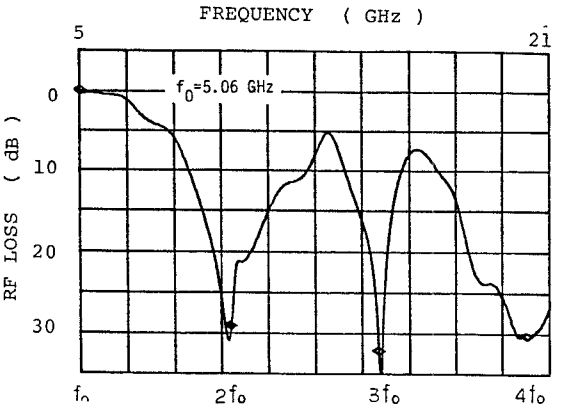



FIG.5 Frequency response of microstrip harmonic rejection filter

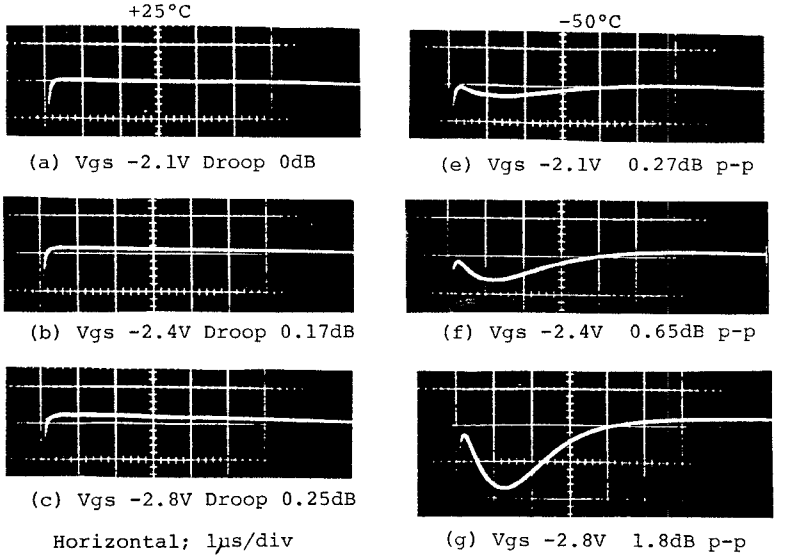



FIG.4 Output RF pulse envelope for three gate-source voltage at 25°C and -50°C of heatsink temperature. 140μF capacitor was connected at drain bias terminal to ground.

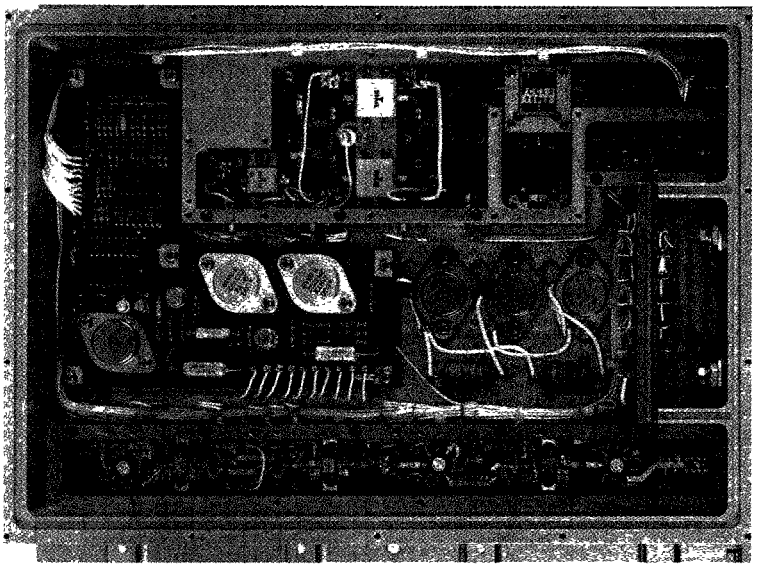


FIG.6 Internal view of the amplifier

of accidental removal of gate bias voltage and extraordinary temperature rise of the amplifier baseplate.

## AMPLIFIER STRUCTURE

Two-way power combiner was realized with microstripline on 0.8mm thick glass reinforced teflon substrate in tolerable losses. Therefore whole microwave circuits were made of microstripline components, and the amplifier was made very simple in structure. The amplifier is 241 x 305 x 70mm in dimensions and 6Kg in weight. The photo is shown in FIG.6. Bottom surface of the amplifier is the thermal interface to the heatsink.

## AMPLIFIER OVERALL PERFORMANCE

The amplifier was tested over the frequency range of 5030 to 5092MHz, RF input power range of +14 to +18dBm and heatsink temperature range of -50 to +70°C . Results are shown in FIG.7.

RF output power was more than 20 watts over above test conditions, and was stabilized within 1dB peak-to-peak variation.

## CONCLUSION

5-GHz 20-watt amplifier for MLS was developed. The output power was obtained from two state-of-the-art high power FETs in the final stage. A GaAs FET limiter with unique input/output characteristics was successfully used to avoid degradation of pulse on/off ratio in the amplifier. Although biasing FETs near pinch-off gate voltage greatly improved the average DC-to-RF conversion efficiency, compromise was required with RF pulse envelope distortion

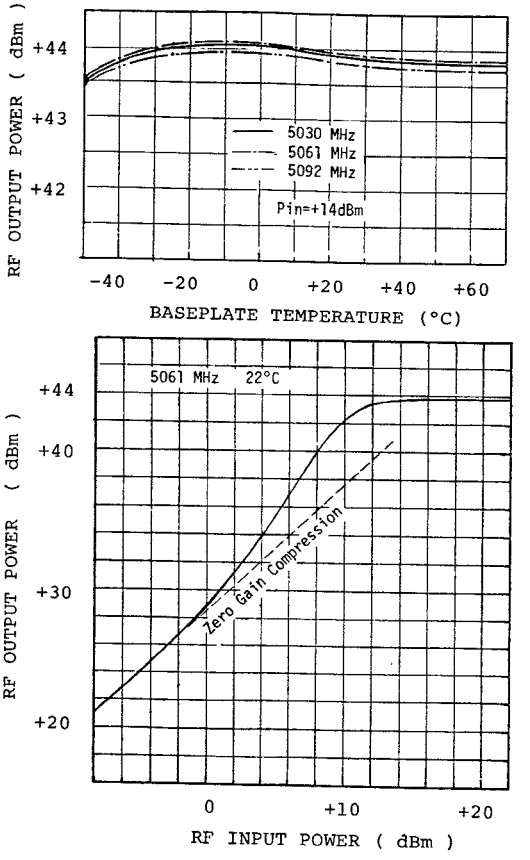



FIG.7 Overall performance of the amplifier

at the leading edge. Open loop control of amplifier gain against temperature change using a PIN attenuator gave stable RF output of within 1dB peak-to-peak variation over the temperature range of -50 to +70°C.

## ACKNOWLEDGEMENT

The authors would like to express their appreciation to Dr.M.Ohtomo, S.Okano and K.Mishima of the encouragement and helpful discussions. They also thank S. Yanagawa for supplying FETs and T.Matsumoto for his significant technacal contribution to the development.

## REFERENCES

(1) S.Yanagawa, Y.Yamada, M.Itoh, K.Arai and N.Tomita, "High Power and High Efficiency Ion-Implanted Power GaAs FETs for C and X Bands", IEEE MTT-S Int.Microwave Symp. Dig., pp332-335

(2) M.Cohn, J.E.Degenford and R.G.Freitag, "Class B Operation of Microwave FETs for Array Module Applications", IEEE MTT-S Int. Microwave Symp. Dig., pp 169-171